Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A pipelined multistreaming processor, comprising:

an instruction ~~source~~cache;

~~a plurality of streams~~fetch logic coupled to said instruction cache enabled to concurrently fetch instructions for a plurality of instruction streams ~~at different times~~ from the instruction ~~source~~cache;

a plurality of instruction queues coupled to said fetch logic where each one of said plurality of instruction queues is associated with at least one of said plurality of instruction streams;

a dispatch stage coupled to said plurality of instruction queues for selecting and dispatching instructions for said plurality of instruction streams to a set of execution units; and

~~a set of instruction queues having one queue associated with each stream in the plurality of streams, and located in the pipeline between the instruction source and the dispatch stage; and~~

~~a select system~~select logic coupled to said instruction cache for selecting ones of said plurality of instruction streams ~~in each cycle~~ to fetch instructions from ~~the~~ said instruction ~~source~~cache.[[;]]

~~wherein the select system selects a number of streams for which to fetch instructions, which are fewer in number than the number of streams in the plurality of streams.~~

2. (Currently amended) The processor of claim 1 wherein the number of said ones of said plurality of instruction streams ~~in the plurality of streams is eight, and the number of streams~~ selected by said select logic for fetching, is less than the number of said plurality of instruction streams. ~~for which to fetch instructions in each cycle is two.~~

3. (Currently amended) The processor of claim 2 wherein ~~the~~ said select ~~system~~ logic monitors a ~~set of fetch~~ plurality of program counters (FPC) ~~having one~~each of said plurality of ~~FPC~~ program counters associated with ~~each~~ one of said plurality of instruction streams, and wherein said select logic directs fetching from said instruction cache ~~if instructions beginning~~ at addresses ~~according to the~~ stored in said plurality of program counters.

4. (Currently amended) The processor of claim 3 wherein said select logic also monitors said plurality of instruction queues and determines said ones of said plurality of instruction streams, for which to fetch, based on how full said plurality of instruction queues are. ~~The processor of claim 2 wherein each stream selected to fetch is directed to fetch eight instructions from the instruction source.~~

5. (Canceled)

6. (Currently amended) The processor of claim 1 wherein ~~the set of execution units comprises eight arithmetic logic units (ALUs), and two memory units.~~ said fetch logic concurrently stores fetched instructions into ones of said plurality of instruction queues that are associated with said ones of said plurality of instruction streams fetched by said fetch logic.

7. (Currently amended) In a ~~pipelined~~ multistreaming processor, the processor ~~having~~executing [[an]]a plurality of instruction ~~queue~~streams, a method for ~~disassociating~~ decoupling fetching of instructions for the plurality of instruction streams from ~~a dispatch stage~~the dispatch of those instructions for execution, the method comprising ~~the steps of~~:

~~(a)~~ placing a ~~set~~ plurality of instruction queues in the processor, one instruction queue for each instruction stream, ~~in the pipeline~~ the plurality of queues located between [[the]]fetch logic, which fetches instructions for the instruction streams, and dispatch logic, which dispatches instructions for the instruction streams;~~instruction source and the dispatch stage;~~ and

~~(b)~~ placing select logic in the processor, the select logic selecting ~~one or more streams, fewer than the number of streams in the multistreaming processor,~~ a plurality of instruction streams for which to fetch instructions ~~in each cycle~~ from an instruction ~~source~~cache, the number of instruction streams selected by the select logic being less than the number of instruction streams in the processor;

wherein by selecting a plurality of instruction streams for fetching which is less than the number of instruction streams executing, the association between fetching of instructions, and their dispatch is effectively decoupled.

8. (Currently amended) The method of claim 7 ~~wherein the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two.~~further comprising:

having the select logic choose which of the instruction streams to fetch based on the contents of the plurality of instruction queues, the select logic choosing to fetch instructions for those instruction streams whose instruction queues are most empty.

9. (Currently amended) The method of claim 8 wherein the select logic further comprises a plurality of fetch program counters, each for storing an address associated with the next instruction to be fetched, for each of the plurality of instruction streams.~~the select system monitors a set of fetch program counters (FPC) having one FPC associated with each stream, and directs fetching if instructions beginning at addresses according to the program counters.~~

10. (Currently amended) The method of claim [[7]]9 wherein the fetch logic utilizes the contents of the plurality of fetch program counters to fetch instructions for the selected plurality of instruction streams. ~~each stream selected to fetch is directed to fetch eight instructions from the instruction source.~~

11. (Currently amended) The method of claim 7 wherein the dispatch ~~stage~~ logic dispatches instructions to a ~~set~~ plurality of execution units.

12. (Currently amended) The method of claim 11 wherein the ~~set~~ plurality of execution units comprises eight arithmetic logic units (ALUs), and two memory ~~ports~~units.